IN THE CLAIMS:

Please cancel claims 2, 16, 20, and 21 without prejudice or disclaimer as to the subject matter contained therein.

Please amend the claims as shown in the following claims listing.

1. (Currently amended) A receiver circuit comprising:

an oscillator circuit including an oscillator configured to generate an oscillator signal, wherein the oscillator signal is divided by a first amount ~~configured~~ to generate a calibration tone and by a second amount to generate a phase locked loop (PLL) reference signal;

a phase locked loop circuit configured to generate a PLL output signal that is phase locked in relation to the PLL reference signal;

a quadrature generator configured to generate quadrature mixer local oscillator (LO) signals derived from the PLL output signal; and

an in-phase/quadrature (IQ) mixer configured to mix the calibration tone with the quadrature mixer LO signals;

a first switch coupled to selectively provide the calibration tone to the IQ mixer during a calibration mode of operation; and

a second switch coupled to selectively provide the PLL reference signal to the phase locked loop circuit during the calibration mode of operation, and to provide a different reference signal to the phase locked loop circuit during a normal mode of operation.

2. (Cancelled)

3. (Currently amended) The receiver circuit as recited in Claim [[2]] 1, wherein during the calibration mode of operation the oscillator is configured to operate near a particular frequency in an open loop mode.

4. (Original) The receiver circuit as recited in Claim 3, wherein the oscillator is a voltage controlled oscillator.

5. (Currently amended) The receiver circuit as recited in Claim 3, wherein the oscillator circuit includes a first divider circuit ~~coupled~~ configured to divide a frequency of the oscillator signal by [[a]] the ~~first~~ second amount to generate the PLL reference signal.

6. (Original) The receiver circuit as recited in Claim 5, wherein the first divider circuit is a power of two ripple divider.

7. (Currently amended) The receiver circuit as recited in Claim 5 further comprising a second divider circuit ~~coupled~~ configured to divide the frequency of the oscillator signal by [[a]] the ~~second~~ first amount to generate the calibration tone.

8. (Original) The receiver circuit as recited in Claim 7 wherein the second divider circuit is a programmable divider.

9-10. (Cancelled)

11. (Currently amended) The receiver circuit as recited in Claim 1, wherein the first switch is further coupled to selectively provide a receiver RF input signal to the IQ mixer during ~~another~~ a normal mode of operation.

12. (Original) The receiver circuit as recited in Claim 11 further comprising an amplifier coupled to amplify the receiver RF input signal prior to mixing in the IQ mixer.

13. (Original) The receiver circuit as recited in Claim 1, wherein the IQ mixer generates an in-phase (I) signal and a quadrature (Q) signal that are conveyed through an I channel and a Q channel, respectively, for processing by a baseband circuit.

14. (Original) The receiver circuit as recited in Claim 13 further comprising a calibration subsystem coupled to receive representations of the in-phase (I) signal and the quadrature (Q) signal, wherein the calibration subsystem is configured to determine one or more correction parameters for canceling a residual image signal.

15. (Original) The receiver circuit as recited in Claim 14 further comprising an analog-to-digital converter coupled to convert the I and Q signals generated by the IQ mixer to digital signals.

16. (Cancelled)

17. (Currently amended) The receiver circuit as recited in Claim [[16]] 5, wherein during another mode of operation the oscillator is coupled to operate as a transmit oscillator within an offset phase locked loop circuit.

18. (Currently amended) A method comprising:

an oscillator circuit including an oscillator generating an oscillator signal, generating a calibration tone by dividing the oscillator signal by a first amount, and a PLL reference signal by dividing the oscillator signal by a second amount;

a phase locked loop circuit generating a PLL output signal that is phase locked in relation to the PLL reference signal;

generating quadrature mixer LO signals dependent upon the PLL output signal; ~~and~~

mixing the calibration tone with the quadrature mixer LO signals;

selectively providing, via a first switch, the calibration tone to the IQ mixer during a calibration mode of operation; and

selectively providing, via a second switch, the PLL reference signal to the phase locked loop circuit during the calibration mode of operation, and a different reference signal to the phase locked loop circuit during a normal mode of operation.

19. (Currently amended) The method as recited in claim 18, further comprising ~~an oscillator of~~ the oscillator ~~circuit~~ operating near a particular frequency in an open loop mode.

20-21. (Cancelled)

22. (Currently amended) A receiver circuit comprising:

an oscillator means including an oscillator for generating a calibration tone and a PLL reference signal;

a phase locked loop circuit generating a PLL output signal that is phase locked in relation to the PLL reference signal;

means for generating quadrature mixer LO signals dependent upon the PLL output signal; and

means for mixing the calibration tone with the quadrature mixer LO signals;

means for selectively providing the calibration tone to the quadrature mixer during a calibration mode of operation; and

means for selectively providing the PLL reference signal to the phase locked loop circuit during the calibration mode of operation, and for providing a different reference signal to the phase locked loop circuit during a normal mode of operation.